mipea Documentation

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CHAPTER 1

Installation

The source code is hosted on GitHub. mipea uses autotools (autoconf, automake, libtool) to build and install the library. So obtaining the library is very easy:

```
$ git clone https://github.com/jasLogic/mipea.git
$ cd mipea
$ ./configure
$ make
$ sudo make install
```

1.1 Troubleshooting

If the `configure` script prints this warning:

```
configure: WARNING: cannot find file /proc/cpuinfo
```

than the script was unable to find the `cpuinfo` file which is needed to determine the SoC (BCM2835 or BCM2836/7) and the revision. Pis with a revision number where the last four digits are less than `0004` use I2C bus 0 instead of 1, like the new ones.

This error can be fixed by editing the `config.h` file ensuring that it contains these lines (depending on your Pi):

```
#define BCM2835         1
#define BCM2836_7       1
#define USE_I2C_BUS_0   1
```

CHAPTER 2

Peripherals

The peripheral functions are something like the *core* of the library. They map and unmap the memory used by all other parts.

2.1 Macros

PERIPHERAL_BASE_BCM2835
This macro holds the value of the peripheral base, when a BCM2835 is used. It has the value `0x20000000`

PERIPHERAL_BASE_BCM2836_7
This macro holds the value of the peripheral base, when a BCM2836 or BCM2837 is used. It has the value `0x3F000000`

2.2 Functions

uint32_t * **peripheral_map** (uint32_t *offset*, uint32_t *size*)
This function maps a code memory block of size `size` at offset `offset` from the peripheral base.

Note: The `offset` must be a multiple of the page size which is `4096` on the Raspberry Pi.

The function returns a pointer to the mapped memory on success and `NULL` on error.

void **peripheral_unmap** (void* *map*, uint32_t *size*)
This function unmaps the memory mapped to pointer `map` with size `size`.

int **peripheral_ismapped** (void **map*, uint32_t *size*)
This function checks if a pointer `map` is already mapped to a memory region with the size `size`. It returns `true` if the pointer is already mapped and `false` if not.

CHAPTER 3

Clock Manager

3.1 Macros

CLOCK_MANAGER_OFFSET
This macro defines the offset at which the clock manager registers are located relative to the peripheral base. It has the value `0x101000`

CLOCK_MANAGER_SIZE
This macro holds the size of the clock manager registers which needs to be mapped. It has the value `0xA4`

CM_PASSWD
This macro holds the clock manager password. This value must always be present when writing to a clock manager register (e.g. by OR with the value). It has the value `0x5A000000`

3.2 Registers

volatile uint32_t ***clock_manager_base_ptr**
This pointer points, when mapped, to the base of the clock manager registers.

struct **clock_manager_register_map**
This struct maps the registers of the clock manager. The names of the struct members correspond to the registers. Unfortunately, the official datasheet does not feature this chapter. But there is an upload of this chapter here: BCM2835 clocks:

```
struct clock_manager_register_map {
    uint32_t GP0CTL;
    uint32_t GP0DIV;
    uint32_t GP1CTL;
    uint32_t GP1DIV;
    uint32_t GP2CTL;
    uint32_t GP2DIV;
    uint32_t: 32;
```

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```
    uint32_t: 32;
    uint32_t: 32;
    uint32_t: 32;
    uint32_t PCMCTL;
    uint32_t PCMDIV;
    uint32_t PWMCTL;
    uint32_t PWMDIV;
}
```

CM

```
#define CM ((volatile struct clock_manager_register_map *)(clock_manager_base_ptr␣
↪+ 28))
```

By using this macro, the registers of the clcok manager can be accessed like this `CM->PWMCTL`.

3.3 Enums

clock_source_t

This enum holds the values for the different clock sources:

```
typedef enum {
    CLOCK_GND,
    CLOCK_OSC,
    CLOCK_TST0,
    CLOCK_TST1,
    CLOCK_PLLA,
    CLOCK_PLLC,
    CLOCK_PLLD,
    CLOCK_HDMI
} clock_source_t;
```

3.4 Functions

uint32_t * **clock_map** (void)

This function maps the clock manager registers. It calls *peripheral_map()* with the values *CLOCK_MANAGER_OFFSET* and *CLOCK_MANAGER_SIZE*.

void **clock_unmap** (void)

This function unmaps the clock manager.

The following functions all take a pointer to a clock manager register as an argument because all the registers for the *different clocks* have the *same structure*. This means that you just need to tell the clock manager which clock to use (by pointing to the right register). For example: `clock_enable(&CM->PWMCTL);`

void **clock_enable** (volatile uint32_t **reg*)

This function enables the clock with the register pointed to by `reg`.

void **clock_disable** (volatile uint32_t **reg*)

This function disables the clock with the register pointed to by `reg`.

void **clock_configure**(volatile uint32_t **reg*, *clock_source_t src*, unsigned int *divisor*, unsigned int *mash*)

This function configures the clock with the register pointed to by `reg` and sets up the *clock_source_t* `src`, the divisor `divisor` with the mash factor `mash`.

Todo: Add a decimal places to the divisor.

CHAPTER 4

GPIOs

4.1 Macros

GPIO_OFFSET
This macro defines the offset at which the GPIO registers are located from the peripheral base. It has the value `0x200000`

GPIO_SIZE
This macro holds the size of the GPIO registers which needs to be mapped. It has the value `0xB0`

4.2 Registers

volatile uint32_t ***gpio_base_ptr**
This pointer points, when mapped, to the base of the GPIO registers.

struct **gpio_register_map**
This struct maps the registers of the GPIOs. The names of the struct members correspond to the registers from the Datasheet:

```
struct gpio_register_map {
        uint32_t FSEL[6];
        uint32_t: 32;
        uint32_t SET[2];
        uint32_t: 32;
        uint32_t CLR[2];
        uint32_t: 32;
        uint32_t LEV[2];
        uint32_t: 32;
        uint32_t EDS[2];
        uint32_t: 32;
        uint32_t REN[2];
        uint32_t: 32;
```

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```
        uint32_t FEN[2];
        uint32_t: 32;
        uint32_t HEN[2];
        uint32_t: 32;
        uint32_t LEN[2];
        uint32_t: 32;
        uint32_t AREN[2];
        uint32_t: 32;
        uint32_t AFEN[2];
        uint32_t: 32;
        uint32_t PUD;
        uint32_t PUDCLK[2];
};
```

GP

```
#define GP ((volatile struct gpio_register_map *)gpio_base_ptr)
```

By using this macro, the registers of the GPIOs can be accessed like this `GP->SET[0]`.

4.3 Enums

pin_functions_t

This enum holds the values for the various pin functions:

```
typedef enum {
        INPUT, OUTPUT, ALT0, ALT1, ALT2, ALT3, ALT4, ALT5
} pin_functions_t;
```

pud_t

This enum holds the values for the states of the pullups / -downs:

```
typedef enum {
        PUD_DISABLE, PUD_DOWN, PUD_UP
} pud_t;
```

4.4 Functions

uint32_t * **gpio_map** (void)

This function maps the GPIO registers. It calls `peripheral_map()` with the values `GPIO_OFFSET` and `GPIO_SIZE`.

void **gpio_unmap** (void)

This function unmaps the GPIOs.

void **gpio_func** (uint32_t *pin*, *pin_functions_t function*)

This function sets the pin `pin` to the pin function `function`.

void **gpio_set** (uint32_t *pin*)

Set the pin `pin`.

void **gpio_clr**(uint32_t *pin*)
: Clear the pin `pin`.

uint32_t **gpio_tst**(uint32_t *pin*)
: Test the pin `pin`. This function returns `0` or `false` when the pin is low and non-zero if the pin is high.

void **gpio_pud**(uint32_t *pin*, *pud_t val*)
: Use the pullup / -down functionality `val` on the pin `pin`.

void **gpio_inp**(uint32_t *pin*)
: Make pin `pin` an input.

void **gpio_out**(uint32_t *pin*)
: Make pin `pin` an output.

void **gpio_clear_pud**(void)
: This function clears all pullup / -downs. This function is called in `gpio_map()` and `gpio_unmap()` because the Raspberry Pi does *not* clear its pullup / -downs, even after power down.

CHAPTER 5

I2C

5.1 Macros

I2C_OFFSET_0

```
0x205000
```

I2C_OFFSET_1

```
0x804000
```

The BCM2835/6/7 has three BSC (I2C) controllers, from which only one is connected to the I2C pins. The older Pis (where the last four digits of the revision number are less than `0004`) have BSC0 connected to the pins, all the other BSC1. The configure script tries to read the `/proc/cpuinfo` file, which includes the revision number, and than defines `USE_I2C_BUS_0` accordingly. See *Installation*

I2C_SIZE
This macro holds the size of the I2C registers which needs to be mapped. It has the value `0x18`

`I2C_FIFO_SIZE I2C_C_I2CEN I2C_C_ST I2C_C_CLEAR I2C_C_READ I2C_S_RXS I2C_S_TXD I2C_S_DONE`

5.2 Registers

volatile uint32_t ***i2c_base_ptr**
This pointer points, when mapped, to the base of the I2C registers.

struct **i2c_register_map**
This struct maps the registers of the BSC controller. The names of the struct members correspond to the registers from the Datasheet:

```
struct i2c_register_map {
    uint32_t C;
    uint32_t S;
    uint32_t DLEN;
    uint32_t A;
    uint32_t FIFO;
    uint32_t DIV;
    uint32_t DEL;
    uint32_t CLKT;
};
```

I2C

```
#define I2C ((volatile struct i2c_register_map *)i2c_base_ptr)
```

By using this macro, the registers of the I2C can be accessed like this `I2C->FIFO`.

5.3 Structs

i2c_config_t

This struct is used to configure the I2C controller:

```
typedef struct {
    uint8_t addr: 7;
    uint16_t div;
    uint16_t clkstr;
} i2c_config_t;
```

uint8_t addr: **7**

This member holds the address of the I2C device that should be contacted. I2C addresses have a length of seven bits.

uint16_t **div**

This member sets the clock divider for the BSC controller.

Note: The clock source is the core clock with a frequency, according to the Datasheet, of `150 MHz` and according to this file and other sources of `250 MHz`. When I tested the clock speed of I2C and SPI with a logic analyzer, it seems that `250 MHz` **is correct** (at least for the Raspberry Pi Zero I use).

uint16_t **clkstr**

This member sets the clock stretch timeout (or delay). This means that the master will wait `clkstr` cycles after the rising clock edge for the slave to respond. After this the timeout flag is set.

5.4 Functions

uint32_t * **i2c_map**(void)

This function maps the I2C registers. It calls *peripheral_map()* with the values `I2C_OFFSET` and *I2C_SIZE*. `I2C_OFFSET` is defined in `i2c.c`.

void **i2c_unmap**(void)

This function unmaps the I2C registers.

void **i2c_configure** (*i2c_config_t *config*)
This function configures the BSC controller with the `i2c_config_t` pointed to by `config`.

void **i2c_start** (void)
Starts the BSC controller and clears the flag register.

void **i2c_stop** (void)
Disables the BSC controller.

void **i2c_write_byte** (uint8_t *byte*)
Write a `byte` of data.

uint8_t **i2c_read_byte** (void)
This function receives a `byte` of data and returns it.

void **i2c_write_data** (const uint8_t **data*, uint16_t *length*)
This function writes `length` bytes of data pointed to by `data`.

void **i2c_read_data** (uint8_t **data*, uint16_t *length*)
This function receives `length` bytes of data and writes them to the array `data`.

void **i2c_write_register** (uint8_t *reg*, uint8_t *data*)
This function writes to bytes of data. First `reg` and then `data`.

Note: You *cannot* use two calls to `i2c_write_byte()` instead of this function because this is only *one* transmission, while two times `i2c_write_byte()` would be *two* different transmissons.

uint8_t **i2c_read_register** (uint8_t *reg*)
In contrast to `i2c_write_register()` you *can* use a call to `i2c_write_byte()` and to `i2c_read_byte()`. This is because I2C needs to make two transmissions anyway to change the read / write bit.

CHAPTER 6

PWM

Note: The Datasheet specifies PWM channels 0 and 1. The Raspberry Pi has pins for PWM channels 1 and 2, you just need to add one.

6.1 Macros

PWM_OFFSET
This macro defines the offset at which the PWM registers are located from the peripheral base. It has the value `0x20C000`

PWM_SIZE
This macro holds the size of the I2C registers which needs to be mapped. It has the value `0x24`

RNG_CHANNEL0

DAT_CHANNEL0

RNG_CHANNEL1

DAT_CHANNEL1

```
#define RNG_CHANNEL0    PWM->RNG1
#define DAT_CHANNEL0    PWM->DAT1
#define RNG_CHANNEL1    PWM->RNG2
#define DAT_CHANNEL1    PWM->DAT2
```

To prevent confusion (because the Datasheet calls the PWM channels 1 and 2 and the Raspberry Pi 0 and 1) the values of the registers which need to be used "on the fly" are :code;'defined' from 2 to 1 and from 1 to 0.

6.1.1 Configuration Macros

PWM_CTL_MODE_PWM	Use PWM mode
PWM_CTL_MODE_SERIALISER	Use serialiser mode
PWM_RPTL_STOP	If serialiser mode: Transmission stops when fifo empty
PWM_RPTL_REPEAT	If serialiser mode: Repeat last data when fifo empty
PWM_SBIT_LOW	Output low when no transmission active
PWM_SBIT_HIGH	Output high when no transmission active
PWM_POLA_DEFAULT	Polarity is default
PWM_POLA_INVERTED	Polarity is innverted
PWM_USEF_DATA	Data register is transmitted
PWM_USEF_FIFO	Data from fifo is transmitted
PWM_MSEN_PWMALGORITHM	Use PWM algorithm
PWM_MSEN_MSRATIO	Use MS ratio

6.2 Registers

volatile uint32_t ***pwm_base_ptr**
This pointer points, when mapped, to the base of the PWM registers.

struct **pwm_register_map**
This struct maps the registers of the PWM. The names of the struct members correspond to the registers from the Datasheet:

```
struct pwm_register_map {
    uint32_t CTL;
    uint32_t STA;
    uint32_t DMAC;
    uint32_t: 32;    // address not implemented
    uint32_t RNG1;
    uint32_t DAT1;
    uint32_t FIF1;
    uint32_t: 32;    // address not implemented
    uint32_t RNG2;
    uint32_t DAT2;
};
```

PWM

```
#define PWM ((volatile struct pwm_register_map *)pwm_base_ptr)
```

By using this macro, the registers of the PWM can be accessed like this `PWM->RNG1`.

6.3 Enums

pwm_channel_t
This enum holds the values distinguishing PWM channel 0 and 1:

```
typedef enum {
    PWM_CHANNEL0, PWM_CHANNEL1
} pwm_channel_t;
```

6.4 Structs

pwm_channel_config_t

This struct is used to configure a PWM channel:

```
typedef struct {
    pwm_channel_t channel;
    union {
        struct {
            uint32_t: 1;
            uint32_t mode: 1;
            uint32_t rptl: 1;
            uint32_t sbit: 1;
            uint32_t pola: 1;
            uint32_t usef: 1;
            uint32_t: 1;
            uint32_t msen: 1;
        };
        uint32_t ctl_register;
    };
    unsigned int divisor;
    uint32_t range;
} pwm_channel_config_t;
```

pwm_channel_t **channel**

This member specifies the PWM channel to configure.

uint32_t **ctl_register**

This member can be directly edited by the anonymous struct inside this union. This register maps directly to the `CTL` register, with some offset for PWM 1. The settings of this register are described in the *Macros*.

unsigned int **divisor**

The divisor which is passed to the *Clock Manager*.

uint32_t **range**

The range to which the PWM counter counts before it starts over.

6.5 Functions

uint32_t * **pwm_map** (void)

This function maps the PWM registers. It calls `peripheral_map()` with the values `PWM_OFFSET` and `PWM_SIZE`.

void **pwm_unmap** (void)

This function unmaps the PWM registers.

void **pwm_configure** (*pwm_channel_config_t *config*)

This function configures a PWM channel with a `pwm_channel_config_t` pointed to by `config`.

void **pwm_enable** (*pwm_channel_t channel*)

This function enables `pwm_channel_t channel`.

void **pwm_disable** (*pwm_channel_t channel*)

This function disables `pwm_channel_t` `channnel`.

CHAPTER 7

SPI

7.1 Macros

SPI_OFFSET
This macro defines the offset at which the SPI registers are located from the peripheral base. It has the value `0x204000`

SPI_SIZE
This macro holds the size of the I2C registers which needs to be mapped. It has the value `0x14`

7.1.1 Configuration Macros

SPI_CS_CE0	Use chip enable 0
SPI_CS_CE1	Use chip enable 1
SPI_CS_CE2	Use chip enable 2
SPI_CPHA_CLK_BEGINNING	Data on clock leading edge
SPI_CPHA_CLK_MIDDLE	Data on clock trailing edge
SPI_CPOL_RESET_LOW	Clock polarity: active low
SPI_CPOL_RESET_HIGH	Clock polarity: active high
SPI_CSPOL_ACTIVE_LOW	Chip enable: active low
SPI_CSPOL_ACTIVE_HIGH	Chip enable: active high

7.2 Registers

volatile uint32_t ***spi_base_ptr**
This pointer points, when mapped, to the base of the SPI registers.

struct **spi_register_map**
This struct maps the registers of the SPI. The names of the struct members correspond to the registers from the Datasheet:

```
struct spi_register_map {
    uint32_t CS;
    uint32_t FIFO;
    uint32_t CLK;
    uint32_t DLEN;
    uint32_t LTOH;
    uint32_t DC;
};
```

SPI

```
#define SPI ((volatile struct spi_register_map *)spi_base_ptr)
```

By using this macro, the registers of the SPI can be accessed like this `SPI->CS`.

7.3 Structs

spi_channel_config_t

This struct is used to configure SPI:

```
typedef struct {
    union {
        struct {
            uint32_t cs: 2;
            uint32_t cpha: 1;
            uint32_t cpol: 1;
            uint32_t: 2;
            uint32_t cspol: 1;
            uint32_t: 14;
            uint32_t cspol0: 1;
            uint32_t cspol1: 1;
            uint32_t cspol2: 1;
        };
        uint32_t cs_register;
    };

    uint16_t divisor;
} spi_channel_config_t;
```

uint32_t **cs_register**

This member can be directly edited by the anonymous struct inside this union. This register maps directly to the `CS` register. The settings of this register are described in the *Macros*.

uint16_t **divisor**

The master clock divisor.

Note: The clock source is the core clock with a frequency, according to the Datasheet, of `150 MHz` and according to this file and other sources of `250 MHz`. When I tested the clock speed of I2C and SPI with a logic analyzer, it seems that `250 MHz` **is correct** (at least for the Raspberry Pi Zero I use).

7.4 Functions

uint32_t * **spi_map** (void)
: This function maps the SPI registers. It calls `peripheral_map()` with the values `SPI_OFFSET` and `SPI_SIZE`.

void **spi_unmap** (void)
: This function unmaps the SPI registers.

void **spi_configure** (*spi_channel_config_t *config*)
: This function configures SPI with a `spi_channel_config_t` pointed to by `config`.

void **spi_transfer_start** (void)
: This function starts a SPI transfer.

void **spi_transfer_stop** (void)
: This function stops the current SPI transfer.

uint8_t **spi_transfer_byte** (uint8_t *data*)
: While there is a SPI transfer active you can call this function as often as needed by the slave, to send and receive. This function needs to be called between `spi_transfer_start()` and `spi_transfer_stop()`, it sends `data` over SPI and asynchronously receives data and *returns* it.

uint8_t **spi_send2_recv1** (uint8_t *data0*, uint8_t *data1*)
: This function writes to bytes of data and than keeps the clock running to receive and return the third byte. `spi_transfer_start()` and `spi_transfer_stop()` *may not* be called when using this function.

CHAPTER 8

GNU General Public License

```
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                       Version 3, 29 June 2007

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menu, a prominent item in the list meets this criterion.

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packaging a Major Component, but which is not part of that Major
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Major Component, or to implement a Standard Interface for which an
implementation is available to the public in source code form.  A
"Major Component", in this context, means a major essential component
(kernel, window system, and so on) of the specific operating system
(if any) on which the executable work runs, or a compiler used to
produce the work, or an object code interpreter used to run it.

  The "Corresponding Source" for a work in object code form means all
the source code needed to generate, install, and (for an executable
work) run the object code and to modify the work, including scripts to
control those activities.  However, it does not include the work's
System Libraries, or general-purpose tools or generally available free
programs which are used unmodified in performing those activities but
which are not part of the work.  For example, Corresponding Source
includes interface definition files associated with source files for
the work, and the source code for shared libraries and dynamically
linked subprograms that the work is specifically designed to require,
such as by intimate data communication or control flow between those
subprograms and other parts of the work.

  The Corresponding Source need not include anything that users
can regenerate automatically from other parts of the Corresponding
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    (including a physical distribution medium), accompanied by a
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    long as you offer spare parts or customer support for that product
    model, to give anyone who possesses the object code either (1) a
    copy of the Corresponding Source for all the software in the
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    product that is covered by this License, on a durable physical
    medium customarily used for software interchange, for a price no
    more than your reasonable cost of physically performing this
    conveying of source, or (2) access to copy the
    Corresponding Source from a network server at no charge.

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    written offer to provide the Corresponding Source.  This
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    only if you received the object code with such an offer, in accord
    with subsection 6b.

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    copy the object code is a network server, the Corresponding Source
    may be on a different server (operated by you or a third party)
    that supports equivalent copying facilities, provided you maintain
    clear directions next to the object code saying where to find the
    Corresponding Source.  Regardless of what server hosts the
    Corresponding Source, you remain obligated to ensure that it is
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CHAPTER 9

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CHAPTER 10

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